T-41-91

BT&D TECHNOLOGIES

DLR1040 Receiver
DLT1040 Transmitter
FIBER OPTIC DATA LINKS

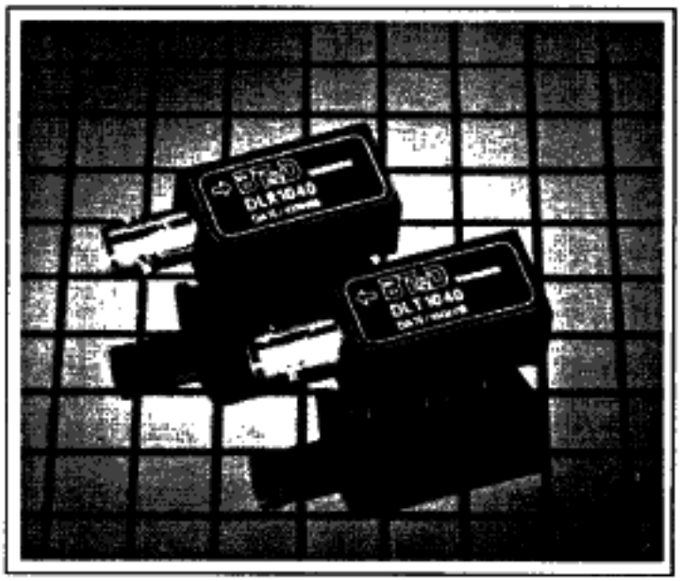
Features:

- Full FDDI
- Single +5-volt power supply
- Compact ST connectorized 16-pin DIP package
- Pin compatible with ODL125*

Applications:

- FDDI Concentrators, Bridges, Routers & Gateways
- Local area networks
- Point-to-point data communications

DL1040



The DL1040 data links are high performance cost efficient modules for serial optical data communications applications with data rates up to 125 Mbd.

These modules are designed for 50 or 62.5 µm core multimode communications fiber and operate at a nominal wavelength of 1310 nm. They incorporate BT&D's high performance, reliable, long wavelength optical devices and proven hybrid technology to give long life and consistent service.

The DLT1040 transmitter uses an advanced edge-emitting (ELED) source which provides exceptional performance on both 62.5 and 50 µm core fibers.

The DLR1040 receiver uses an MOVPE grown planar PIN Photodetector for low dark current and excellent responsivity.

A pseudo-ECL logic interface simplifies interface to FDDI physical layer chip sets.

GENERAL DESCRIPTION

The DL1040 data link modules are designed to provide a simple interface between Pseudo-ECL (PECL)[1] logic and multi-mode optical fiber. The devices are pin compatible with AT&T's ODL125® line of data link components.

The modules are asynchronous having no internal clock recovery or regeneration. This allows the DL1040 to operate in pulse-time modulated analog transmission systems (PFM & PPM) as well as in digital applications.

The PECL interface is used to simplify connection to a number of commercially available products such as Motorola's MC68836 FCG chip or AMD's TAXI™ and SuperNet™ chipsets. The DL1040 is optimized for 125 Mbd operation, but can be used over a range of signal rates. The DL1040 data link set is guaranteed to meet FDDI PMD specifications when used within the operating conditions specified in this document.[2]

Figure 1 - Simplified Transmitter Schematic

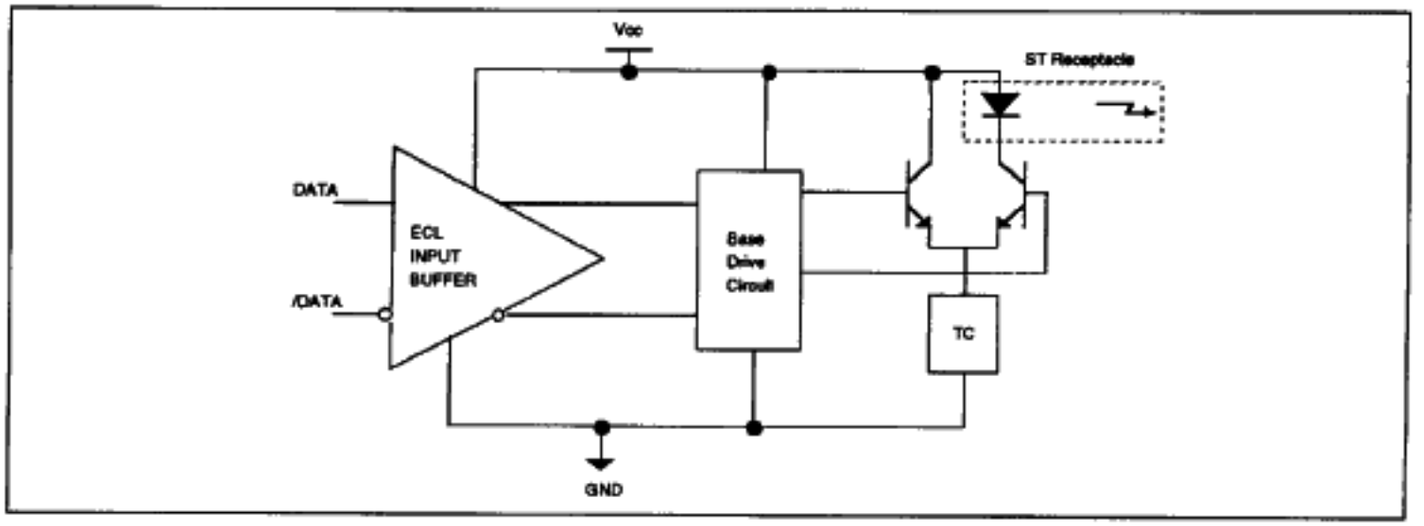
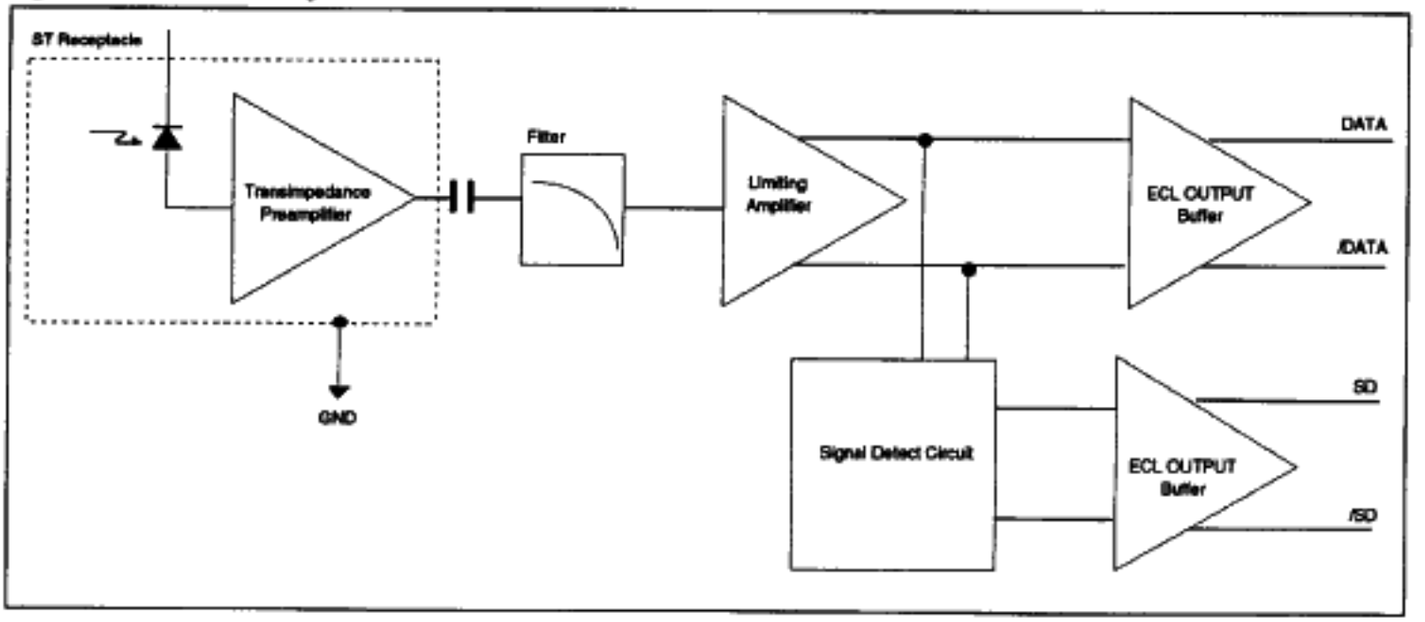
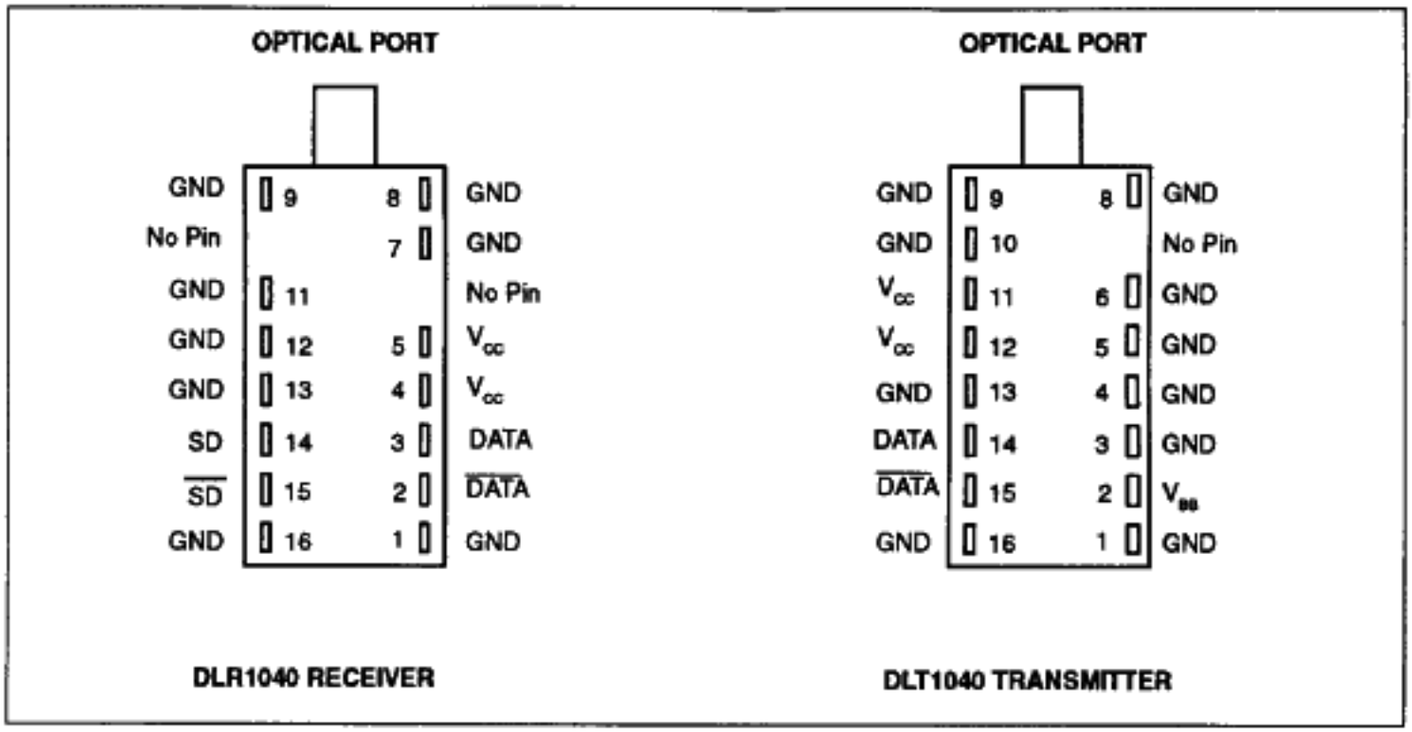


Figure 2 - Receiver Block Diagram



1. Pseudo-ECL Logic is ECL Logic operated from +5V power supplies.
2. FDDI PMD is American National Standard x3.148.

CONNECTION DIAGRAMS - TOP VIEW



GND: Ground connections
These pins are to be connected to the system digital ground (usually 0V). The pins are not all internally connected to each other, but should be connected together on the system board.

SD, $\overline{SD}$: Signal Detect Outputs
These pins are PECL outputs. SD is HIGH when sufficient optical power is present at the input port. This function is defined in PMD section 6.1.1.

V_{cc}: Positive power supply pins
These pins are to be connected to the nominal +5V power supply.

DATA, $\overline{DATA}$: Serial data outputs
These pins are PECL outputs. Data is HIGH during an optical pulse at the receiver input.

GND: Ground connections
These pins are to be connected to the system digital ground (usually 0V).

V_{cc}: Positive power supply pins
These pins are to be connected to the nominal +5V power supply.

DATA, $\overline{DATA}$: Serial data inputs
These pins are PECL differential inputs. When Data is HIGH relative to /DATA, the optical source is turned on. For single-ended data sources, either input can be connected to V_{bb}.

V_{bb}: PECL input bias source
This pin provides a mid-swing reference voltage. It can be used to bias one transmitter input if a single-ended data source is to be used. V_{bb} is nominally 1.29 volts below V_{cc}.

FUNCTIONAL DESCRIPTION DLR1040 RECEIVER

Design

The DLR1040 receiver contains an InGaAs/InP photo detector, a silicon bipolar IC preamplifier and a hybrid postamp/ decision circuit. The preamp and photodetector are mounted in a hybrid sub-assembly to minimize stray capacitance and to provide shielding. This technique yields a highly reliable, but also high performance, receiver module.

The postamplifier is AC- coupled to the preamplifier as illustrated in Figure 2. The coupling capacitor is large enough to pass 4B5B FDDI coded data at 125 Mbd without significant distortion or performance penalty. If a lower signal rate, or a code which has significantly more low frequency content is used, sensitivity, jitter and pulse distortion can be degraded.

Figure 2 also shows a filter network which limits the bandwidth of the preamp output signal. The filter is designed to bandlimit the preamp output noise and thus improve the receiver sensitivity. These components will also reduce the sensitivity of the receiver as the signal bit rate is increased above 125 Mbd.

Noise Immunity

The BT&D receiver includes internal circuit components to filter power supply noise. Testing has shown excellent rejection of power supply noise in the frequency range of 0 to 100 kHz (the range where filter circuit elements become physically large). In addition, rejection of EMI has been tested from 10 kHz to 1 GHz at a field strength of 3V/m with negligable performance degradation.

Under some conditions of EMI and power supply noise, power supply filtering may be necessary. If receiver sensitivity is found to be degraded by power supply noise, the filter network illustrated in Figure 3 may be used to improve performance. The values of the filter components are recommendations and may be changed to suit a particular system environment. Shielded inductors are recommended.

Terminating the Outputs

The PECL Data outputs of the receiver may be terminated with the standard Thevenin-equivalent 50 ohm to V_{cc} -2V terminations shown in Figure 4. Other standard ECL terminating techniques may be used. The two outputs of the receiver should be terminated with identical load circuits to avoid unecessarily large AC current in V_{cc}. If the outputs are loaded identically, the AC current is largely nulled.

The SD outputs of the receiver are PECL logic and must be loaded if they are to be used. Either or both of the outputs may be used. The signal detect circuit is much slower than the data path, so the AC noise generated by an asymmetrical load is negligible. Power consumption may be reduced by using a higher than normal load impedance for the SD outputs. Transmission line effects are not generally a problem as the switching rate is slow.

The Signal Detect Circuit

The signal detect circuit works by sensing the peak level of the received signal and comparing this level to a reference. The signal detect switching levels comply with the FDDI PMD specification over the specified operating temperature and signal pattern.

The DL1040 modules are designed to be wave soldered onto a printed wiring board. It is, however, important to keep fluids and dirt out of the optical port during these and subsequent operations. BT&D can supply a process cap which will allow the part to be used in aqueous or solvent based flux removal systems. Contact your BT&D sales representative for ordering information.

FUNCTIONAL DESCRIPTION DLT1040 TRANSMITTER

Design

The DLT1040 transmitter uses a highly reliable ELED as its optical source. The ELED has the advantage of a narrow numerical aperature. Thus it can couple almost as much light into a 50 µm core fiber as it can into 62.5 µm core fiber. The optical output is obtained by modulating the current in the ELED with a hybrid differential bipolar drive circuit. This circuit includes current pulse shaping and temperature compensation circuitry which optimizes the output pulse shape. Figure 1 shows a block diagram of the transmitter circuits.

The transmitter is DC coupled throughout and thus it can be used with any data pattern or data rate from DC to125 Mbd.

Thermal Performance

The output power of the transmitter varies with temperature with a temperature coefficient <1%/°C. This variation is caused by thermal changes in the conversion efficiency of the ELED. Internal temperature compensation of the ELED drive current tends to stabilize the output power, but design trade-offs require that some residual fluctuation remains.

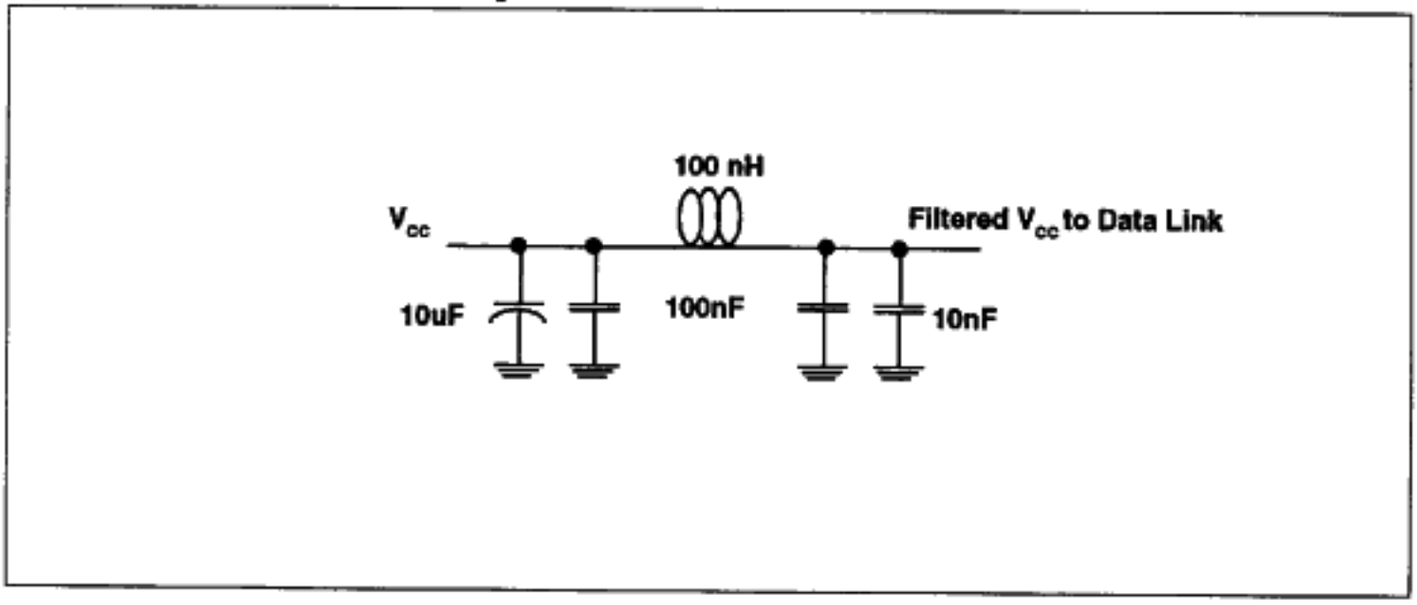
Single-Ended Operation

The transmitter provides a V_{ee} output which is familiar to users of ECL logic. V_{ee} is a reference voltage of 1.29 V below V_{cc} (nominally 3.71 V above ground). This voltage is half-way between a PECL HIGH and a PECL LOW. It can thus be used to bias one of the differential Data inputs if the signal source available is single-ended. It is important to note that PECL logic is referenced to the positive power supply (V_{cc}) and has no rejection of noise on that node. Thus if a single-ended, ground-referenced signal source is used, power supply noise coupled to V_{ee} may exceed the allowable ECL logic noise margin.

Product Safety Notes

Optical Hazards - The DLT1040 optical output cannot present an eye hazard. Good safety practices suggest however, that personnel should not look directly into an optical port during testing or servicing. This avoids hazards resulting from misidentifying a high power optical port.

Figure 3 - π Filter Network for Noise Filtering



MAXIMUM RATINGS

Parameter	Symbol	Minimum	Maximum	Units
Storage Temperature	T_s	-40	+85	°C
Lead Soldering Temperature / Time			240/10	°C/s
Relative Humidity	RH		non-condensing	%RH
Vbb Output Current		-1	+1	mA
Output Current (other outputs)	I_{OUT}	0	30	mA
Input Voltage		V_{EE}	V_{CC}	V
Power Supply Voltage	V_{CC}	0	6	V

OPERATING ENVIRONMENT

Power Supply Voltage	V_{CC}	+4.5	+5.5	V
Ambient Operating Temperature Commercial Industrial	T_{OP}	 0 -40	 70 85	°C

DLT1040 TRANSMITTER PERFORMANCE SPECIFICATIONS

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Center Wavelength		1270	1300	1380	nm
Output Spectral Width			80	120	nm
Optical Output Power [1] Commercial Industrial		-19.0 -23.0	-15.5 -16.5	-14.0 -14.0	dBm dBm
Optical Rise and Fall Time [2]		0.6	2	3.5	ns
Duty Cycle Distortion				0.6	ns
Extinguished Optical Power [3]		0		30	nW
Input Sensitivity [4]			100	300	mV
Input Current (High) [5]			50		uA
Vbb Output Voltage [6]			-1.3		V
Power Supply Current [7]			125	160	mA

PHYSICAL PROPERTIES

Lead Finish	PB/Sn Solder Coat
Weight	10g nominal
Vibration (non op)	MIL-STD-883C, Method 2007A; 4 cycles per axis @ 20G
Shock (non op)	MIL-STD-883C, Method 2002B; 500G, 5 cycles per orientation
ESD	Class 2 per MIL-STD-883 METHOD 3015

DLR1040 RECEIVER PERFORMANCE SPECIFICATIONS

Parameter	Symbol	Minimum	Typical	Maximum	Units
Intput Center Wavelength	λ_C	1270	1300	1380	nm
Sensitivity [8]	sens		-35.5	-33.0	dBm
Maximum Input Power	P_{OPT}	-14.0			dBm
Input Pulse Width		5		1000	ns
Input Duty Cycle [9]		40	50	60	%
Pulse Width Distortion	PWD			0.7	ns_{p-p}
Power to Assert SD [10]	P_{SDA}			-31	dBm
Error rate for SD De-assert [11]				0.01	Errors/Bit
SD Output Hysteresis		1.5			dB
SD Output Assertion Time	t_{SDA}			100	us
SD Output De-assertion Time	t_{SDD}			350	us
Output High Voltage [12]	V_{OH}	-1.0		-0.7	V
Output Low Voltage [12]	V_{OL}	-2.0		-1.6	V
Output Rise/Fall Time	t_R, t_F	0.5	1	1.5	ns
Power Supply Current [13]	I_{CC}	80	100	120	mA

NOTES:

[1] Output power temperature sensitivity is typically <1% per °C. Maximum and minimum values include this variation. Output power specified with 50% duty cycle data, 62.5mm core, 0.275 NA fiber. Industrial temperature range specs are for reference only.

[2] Optical rise and fall times are measured 10 to 90% on a 12.5 MHz square wave signal.

[3] Extinguished optical power is measured with /DATA HIGH and DATA LOW.

[4] Input sensitivity is the voltage difference at the inputs required to switch the optical output state.

[5] HIGH input state is defined as the input pin having voltage at least 300 mV more positive than its complement.

[6] Specified with no load current. Measured w.r.t. V_{CC}.

[7] The power supply current varies with temperature. Maximum current is specified at V_{CC} = +5.5V @ 85°.

[8] Sensitivity is measured with the FDDI Appendix B test pattern. Both DATA and /DATA are PECL terminated. Under 1.38kHz BLW conditions, a minimum sensitivity of -31.0 dBm is specified for DLR1040.

[9] Specifications assume a long-term 50% duty cycle.

[10] This is the maximum power below which SD may be de-asserted.

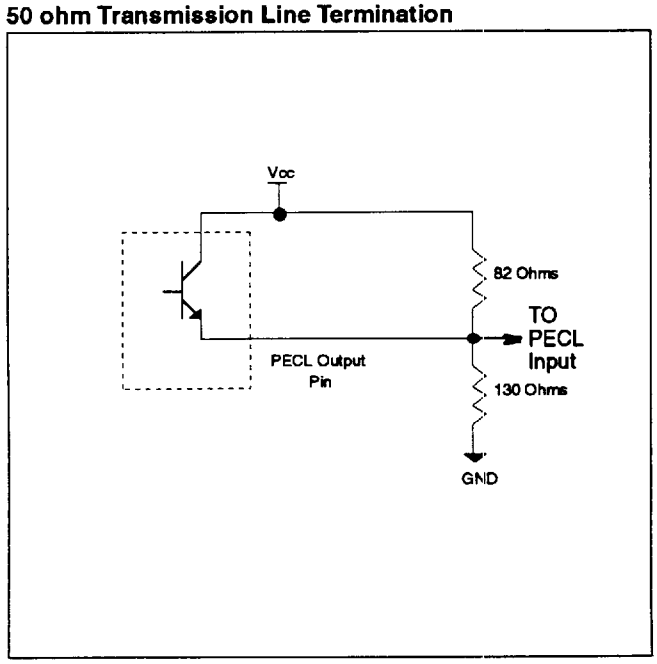
[11] This is the maximum error rate at which SD may remain asserted.

[12] These voltages are measured w.r.t. V_{CC}.

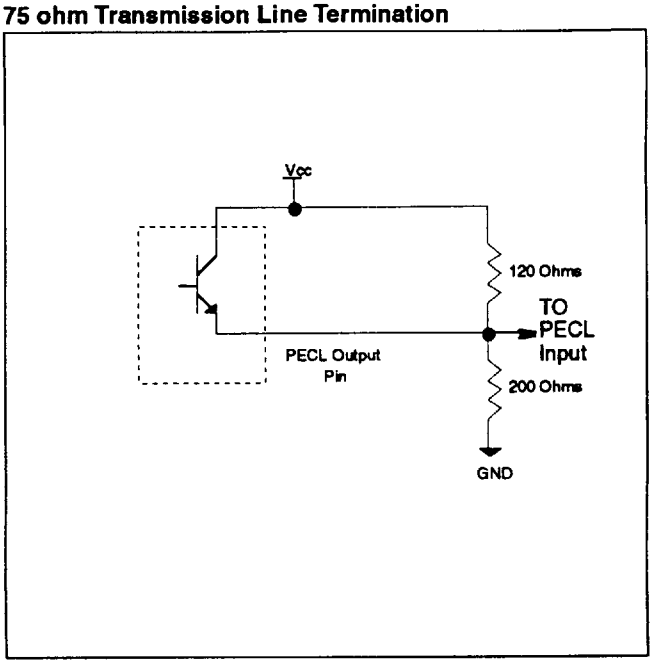
[13] The current excludes the output load current.

PECL OUTPUT TERMINATIONS- FIGURE 4

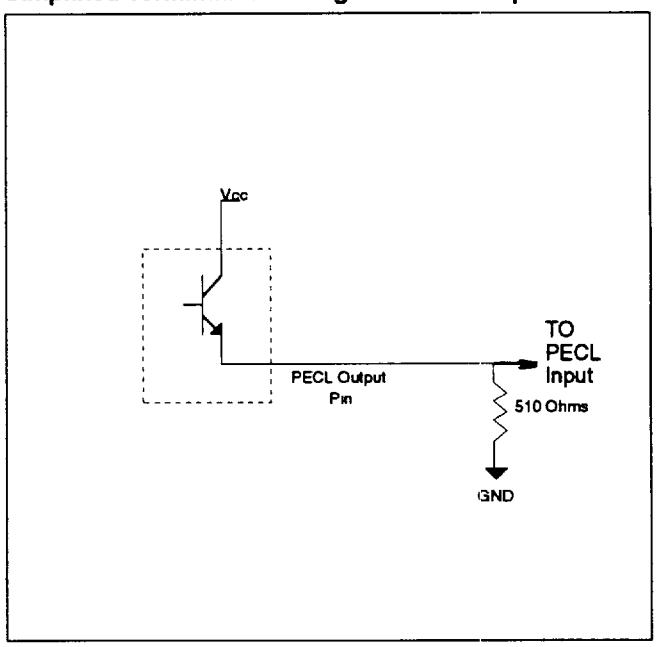
50 ohm Transmission Line Termination



75 ohm Transmission Line Termination



Simplified Termination for Signal Detect Outputs

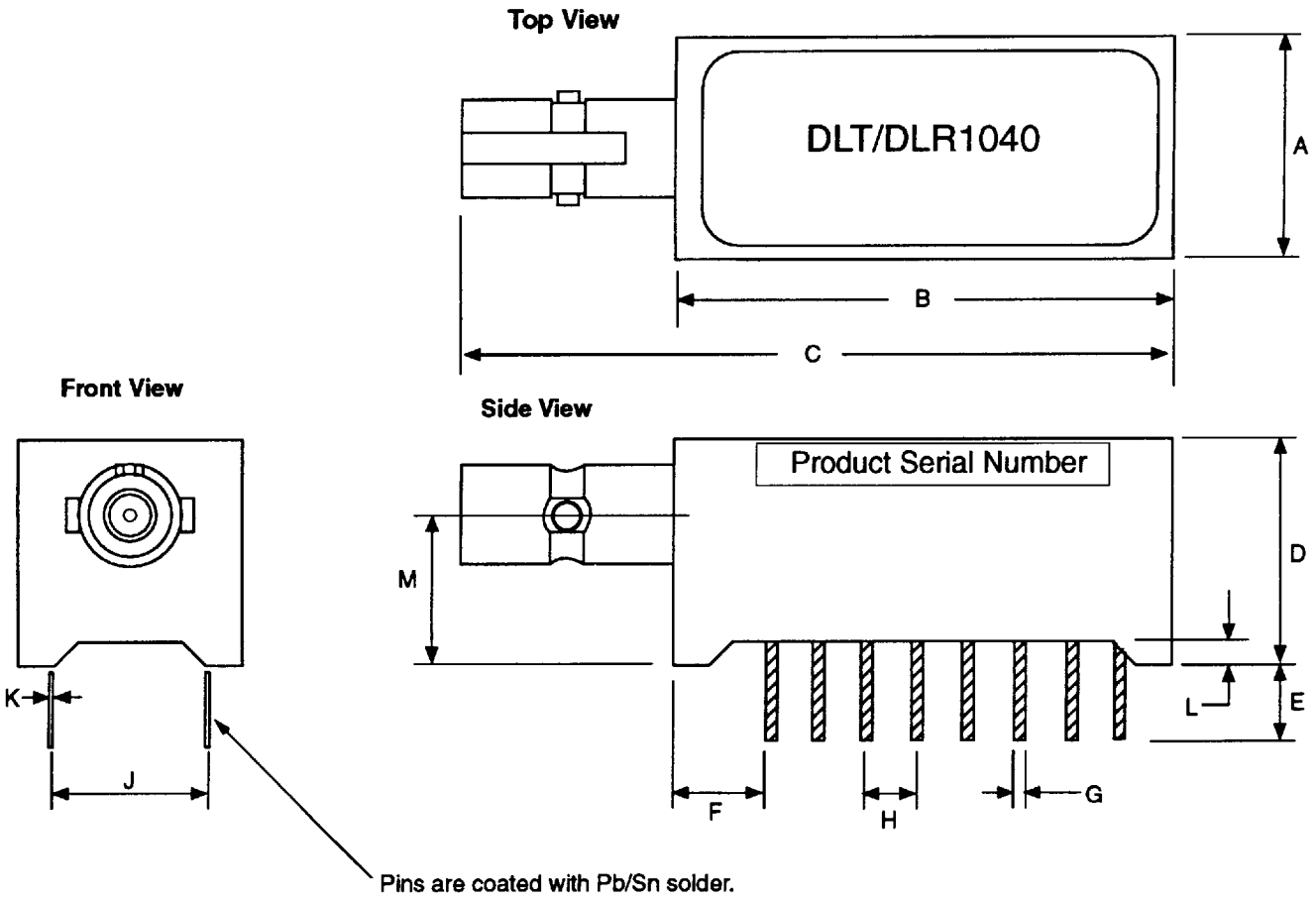


The Figures above give recommended PECL output terminations. The simplified termination consumes about half the power of the other two techniques. Its impedance is too high to match a practical microstrip transmission line and thus it should only be used in situations where the line length is short relative to the signal propagation velocity. For standard FR-4 epoxy-glass board this length is about 5 cm.

PACKAGE DRAWING DL1040

DIM	MIN	NOM	MAX
A	———	———	13.70
B	———	———	25.80
C	———	———	39.00
D	———	———	11.90
E	3.00	———	4.00
F	3.20	———	3.55
G	———	0.50	———
H	———	2.54	———
J	———	7.62	———
K	———	0.38	———
L	———	1.00	———
M	———	7.00	———

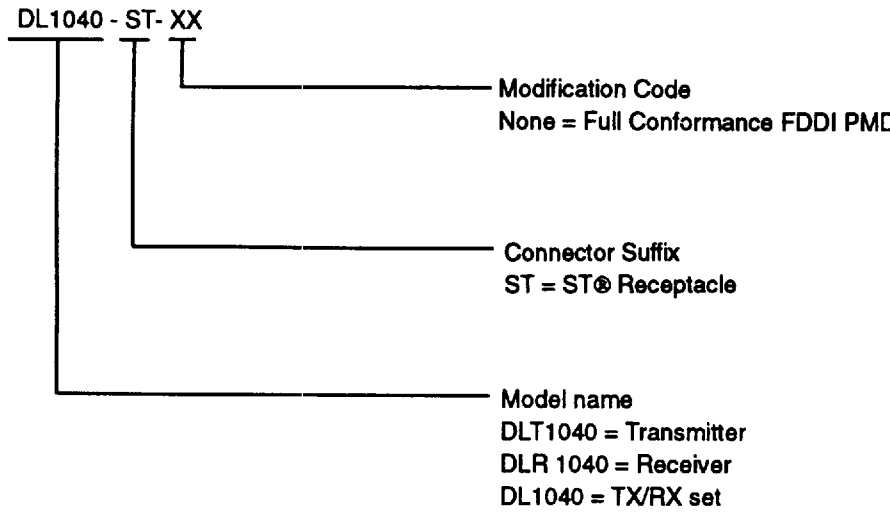
All dimensions in mm



ORDERING INFORMATION

The DL1040 modules may be ordered individually, or as a transmitter/receiver set.

When ordering, please specify the part number as indicated below:



Allowable part number table;
DLT1040 - ST
DLR1040 - ST
DL1040 - ST

HANDLING PRECAUTIONS

The DL1040 can be damaged by current surges or overvoltage. Power supply transient precautions should be taken. Normal handling precautions for electrostatic sensitive devices should be taken.

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(800) 848-1923 (U.S. only)

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